What is claimed is:

1. A method of forming a random-access memory, comprising the steps of:

fabricating a memory circuit on a first substrate;

fabricating a memory controller circuit on a second substrate; and

bonding the first and second substrates to form interconnects between the memory circuit and the memory controller circuit, neither the first substrate alone nor the second substrate alone being sufficient to provide random access data storage.

2. The method of Claim 1, wherein said bonding is thermal diffusion bonding of the first substrate to the second substrate to form a stacked IC structure.

3. The method of Claim 2, wherein at least some of said interconnects are fine-grain vertical interconnects having a pitch of less than 100μm.

4. The method of Claim 3, comprising the step of further bonding the stacked IC structure and a further substrate.

5. The method of Claim 4, wherein said further bonding is thermal diffusion bonding of the stacked IC structure and the further substrate to one another.

6. The method of Claim 5, wherein said thermal diffusion bonding uses fine-grain contact patterns having a contact pitch of less than 100μm.

7. The method of Claim 6, wherein said fine-grain contact patterns form extensions of the fine-grain vertical interconnects.

8. The method of Claim 1, comprising the step of further bonding the stacked IC structure and a further substrate.

9. The method of Claim 8, wherein said further bonding is wire bonding of a singulated stacked IC structure and the further substrate.

10. The method of Claim 1, wherein at least some of the interconnects are formed by a planar process.

11. The method of Claim 8, wherein said further bonding is thermal diffusion metal bonding of fine-grain vertical interconnect contact pattern of a singulated stacked IC structure and the further stacked IC or conventional circuit IC.

12. The method of Claim 8, wherein said further bonding is thermal diffusion metal bonding of an interconnect contact pattern of a singulated stacked IC structure and the further stacked IC or conventional circuit IC.

13. The method of Claim 11, wherein the first and second substrates are wire bonded to a third substrate.

14. The method of Claim 1, wherein said bonding is thermal diffusion bonding of the first substrate to the second substrate to form a stacked IC structure, the method comprising the further steps of:

fabricating at least one additional memory circuit on at least one additional substrate; and

bonding the at least one additional substrate to the stacked IC substrate and forming interconnects between the at least one additional memory circuit and the memory controller circuit, wherein at least some of the interconnects pass through a substrate on which a memory circuit is formed.

15. The method of Claim 14, further comprising the step of:

thinning substrates on which memory circuits are formed to form thinned substrates, facilitating formation of said interconnects.

16. The method of Claim 15, wherein at least some of said interconnects are fine-grain vertical interconnects having a pitch of less than 100μm.

17. The method of Claim 15, wherein said thinned substrates are thinned to less than 50μm in thickness.

18. The method of Claim 15, wherein semiconductor portions of the thinned substrates are thinned to a thickness in the range of about 1-8μm.

19. The method of Claim 15, wherein said thinning comprises grinding said substrates.

20. The method of Claim 19, wherein said substrates are ground subsequent to being bonded.

21. The method of Claim 19, wherein said substrates are ground prior to being bonded.

22. The method of Claim 14, wherein at least one memory circuit is formed on a reusable substrate, further comprising the step of separating a layer in which the memory circuit is formed from the reusable substrate.

23. The method of Claim 22, wherein the at least one memory circuit is formed of polysilicon transistors.

24. The method of Claim 14, wherein bonding comprises thermal diffusion bonding.

25. The method of Claim 24, wherein mating contact patterns are formed on respective surfaces to be bonded together.

26. The method of Claim 25, wherein said mating contact patterns are formed predominantly of metal.

27. The method of Claim 26, wherein said metal includes metal selected from a group consisting of: Al, Sn, Ti, In, Pb, Zn, Ni, Cu, Pt and Au, and alloys thereof.

28. The method of Claim 14, wherein said memory circuits and said memory controller circuit are semiconductor circuits, and wherein the memory controller circuit is fabricated using a first semiconductor process technology and the memory circuits are formed using a second distinct semiconductor process technology.

29. The method of Claim 28, wherein the first semiconductor process technology employs active semiconductor devices of both a first type and a second complementary type.

30. The method of Claim 28, wherein semiconductor devices formed in accordance with the second semiconductor process technology include MOS semiconductor devices, the MOS semiconductor devices all being of a single type.

31. A method of information processing using a stacked integrated circuit memory including a memory controller layer and multiple memory layers, the method comprising the steps of:

initiating a memory access; and

independently routing data vertically between the memory controller layer and selected storage locations within each of a plurality of equal-

size memory blocks.

32. The method of Claim 31, comprising the further steps of:

during a single memory access, accessing data from multiple memory layers.

33. The method of Claim 32, wherein data from one memory layer is used instead of data from another memory layer having a defective portion.

34. The method of Claim 32, wherein data from one memory layer is used to perform ECC processing with respect to data from another memory layer.

35. The method of Claim 31, comprising the further steps of:

receiving within the memory controller layer data from the selected storage locations; and

for each selected storage location, distinguishing between at least four voltage levels to produce at least two bits of data.

36. The method of Claim 31, comprising the further steps of:

receiving data within the memory controller layer; and

decompressing the data.

37. The method of Claim 31, comprising the further steps of:

compressing data within the memory controller layer; and

writing the data to the selected memory locations.

38. A stacked integrated circuit memory comprising:

a first substantially rigid substrate having formed thereon one of a memory circuit and a memory controller circuit; and

at least one substantially flexible substrate having formed thereon the other of said memory circuit and said memory controller circuit and

being bonded to the first substrate.

39. The apparatus of Claim 38, wherein the first substrate has formed thereon the memory circuit and is part of a stack of memory circuit substrates, and the second substrate has formed thereon the memory controller circuit.

40. The method of Claim 39, wherein the first and second substrates are singulated die, the second substrate having greater area than the first substrate.

41. The method of Claim 40, wherein the second substrate has formed thereon additional circuitry separate from the memory controller circuit.

42. The method of Claim 41, wherein the additional circuitry is part of a graphics display subsystem.

43. The method of Claim 41, wherein the additional circuitry comprises a microprocessor.

44. The apparatus of Claim 38, wherein the substantially flexible substrate includes memory I/O pads.

45. The apparatus of Claim 44, wherein the memory circuit is formed proximate a top surface of the flexible substrate, the top surface being bonded to the first substrate, and the memory I/O pads are formed proximate an opposite bottom surface of the flexible substrate.

46. The apparatus of Claim 38, wherein the memory circuit and the memory controller circuit are coupled by vertical interconnects.

47. The apparatus of Claim 46, wherein said vertical interconnects include fine-grain vertical interconnects formed at a pitch of less than 100μm.

48. The method of Claim 47, wherein at least some of the fine-grain vertical interconnects are arrayed in two dimensions.

49. The apparatus of Claim 47, wherein said memory circuit comprises a two-dimensional array of memory blocks, each memory block having formed proximate thereto an array of fine-grain vertical interconnects forming a first port coupling the memory block to the memory controller.

50. The apparatus of Claim 49, wherein at least some memory blocks have formed proximate thereto an array of fine-grain vertical interconnects forming a second port coupling the memory block to the memory controller.

51. The apparatus of Claim 38, wherein at least one of said memory circuits provides redundant memory locations.

52. The apparatus of Claim 51, further comprising an additional substantially flexible substrate on which is formed a redundant memory circuit.

53. The apparatus of Claim 52, wherein the memory controller circuit comprises ECC logic and is programmed to store ECC syndromes in the redundant memory circuit.

54. The apparatus of Claim 51, wherein the memory controller circuit comprises logic for testing the memory circuit.

55. The apparatus of Claim 54, wherein the memory controller circuit is programmed to substitute redundant memory locations for defective memory locations in the memory circuit.

56. The apparatus of Claim 38, wherein the memory controller circuit comprises logic for performing at least one of the following functions: virtual

memory management, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management, and database processing.

57. The apparatus of Claim 38, further comprising a second substrate having formed thereon a redundant memory controller, bonded to the substantially flexible substrate.

58. The apparatus of Claim 38, further comprising a second substrate having formed thereon a microprocessor, bonded to the substantially flexible substrate.

59. The apparatus of Claim 38, wherein the memory controller circuit comprises sense amplifiers coupled to data lines of the memory circuit.

60. The apparatus of Claim 59, wherein the sense amplifiers discriminate between more than two signal levels, each sense amplifier producing a multi-level output signal.

61. The apparatus of Claim 59, wherein the sense amplifiers are sized so as to exhibit a switching speed of about 10ns or less.

62. A method of bonding together multiple substrates each having integrated circuits formed thereon to form interconnections between the integrated circuits, the method comprising the steps of:

processing a mating surface on each of first and second substrates to achieve substantial planarity of the mating surfaces;

forming mating, fine-grain interconnect patterns on the mating surfaces; and

performing fine-grain, planar thermal diffusion bonding of the mating surfaces.

63. The method of Claim 62, wherein said thermal diffusion bonding of the first substrate to the second substrate forms a stacked IC structure.

64. The method of Claim 63, wherein at least some of said interconnects are fine-grain vertical interconnects having a pitch of less than 100μm.

65. The method of Claim 64, comprising the step of further bonding the stacked IC structure and a further substrate.

66. The method of Claim 65, wherein said further bonding is thermal diffusion bonding of the stacked IC structure and the further substrate to one another.

67. The method of Claim 66, wherein said thermal diffusion bonding uses fine-grain contact patterns having a contact pitch of less than 100μm.

68. The method of Claim 67, wherein said fine-grain contact patterns form extensions of the fine-grain vertical interconnects.

69. The method of Claim 62, comprising the step of further bonding the stacked IC structure and a further substrate.

70. The method of Claim 69, wherein said further bonding is wire bonding of a singulated stacked IC structure and the further substrate.

71. The method of Claim 62, wherein at least some of the interconnects are formed by a planar process.

72. The method of Claim 69, wherein said further bonding is thermal diffusion metal bonding of fine-grain vertical interconnect contact pattern of a singulated stacked IC structure and the further stacked IC or conventional circuit IC.

73. The method of Claim 69, wherein said further bonding is thermal diffusion metal bonding of an interconnect contact pattern of a singulated stacked IC structure and the further stacked IC or conventional circuit IC.

74. The method of Claim 72, wherein the first and second substrates are wire bonded to a third substrate.

75. The method of Claim 62, further comprising the step of:

thinning said substrates on which said integrated circuits are formed to form thinned substrates, facilitating formation of said interconnects.

76. The method of Claim 75, wherein at least some of said interconnects are fine-grain vertical interconnects having a pitch of less than 100μm.

77. The method of Claim 75, wherein said thinned substrates are thinned to less than 50μm in thickness.

78. The method of Claim 75, wherein semiconductor portions of the thinned substrates are thinned to a thickness in the range of about 1-8μm.

79. The method of Claim 75, wherein said thinning comprises grinding said substrates.

80. The method of Claim 79, wherein said substrates are ground subsequent to being bonded.

81. The method of Claim 79, wherein said substrates are ground prior to being bonded.

82. The method of Claim 74, wherein at least one integrated circuit is formed on a reusable substrate, further comprising the step of separating a layer in which the integrated circuit is formed from the reusable substrate.

83. The method of Claim 82, wherein the at least one integrated circuit is formed of polysilicon transistors.

84. The method of Claim 74, wherein bonding comprises thermal diffusion bonding.

85. The method of Claim 84, wherein mating contact patterns are formed on respective surfaces to be bonded together.

86. The method of Claim 85, wherein said mating contact patterns are formed predominantly of metal.

87. The method of Claim 86, wherein said metal includes metal selected from a group consisting of: Al, Sn, Ti, In, Pb, Zn, Ni, Cu, Pt and Au, and alloys thereof.